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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/735,517

12/11/2003

Gernot Eckstein

S0193.0011

1592

32172

7590

10/10/2007

DICKSTEIN SHAPIRO LLP

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NEW YORK, NY 10036-2714

EXAMINER

JOHNSON, CARLTON

ART UNIT

PAPER NUMBER

2136

MAIL DATE

DELIVERY MODE

10/10/2007

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

**Advisory Action**  
**Before the Filing of an Appeal Brief**

Application No.

10/735,517

Applicant(s)

ECKSTEIN ET AL.

Examiner

Carlton V. Johnson

Art Unit

2136

**--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

THE REPLY FILED 24 September 2007 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:

- a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.  
b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**NOTICE OF APPEAL**

2. ☐ The Notice of Appeal was filed on \_\_\_\_\_. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

**AMENDMENTS**

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because  
(a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);  
(b) ☐ They raise the issue of new matter (see NOTE below);  
(c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or  
(d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

NOTE: \_\_\_\_\_. (See 37 CFR 1.116 and 41.33(a)).

4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).  
5. ☐ Applicant's reply has overcome the following rejection(s): \_\_\_\_\_.  
6. ☐ Newly proposed or amended claim(s) \_\_\_\_\_ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).  
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☒ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.  
The status of the claim(s) is (or will be) as follows:  
Claim(s) allowed: \_\_\_\_\_.  
Claim(s) objected to: \_\_\_\_\_.  
Claim(s) rejected: 1-10.  
Claim(s) withdrawn from consideration: \_\_\_\_\_.

**AFFIDAVIT OR OTHER EVIDENCE**

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).  
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing of good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).  
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

**REQUEST FOR RECONSIDERATION/OTHER**

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because:  
See Continuation Sheet.  
12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08) Paper No(s). \_\_\_\_\_.  
13. ☐ Other: \_\_\_\_\_.

Continuation of 11. does NOT place the application in condition for allowance because: Response to Remarks

The Kash prior art discloses all claimed actions that must be taken from an external observation standpoint of an integrated circuit in order to defeat attempts to discover the internal operation(s) of the integrated circuit. (see Kash col. 7, lines 37-44: IC (integrated circuit); col. 3, line 66 - col. 4, line 3; col. 4, lines 8-13: time varying electrical (i.e. voltage supply) changes, prevent external detection of IC operation) By definition, an asynchronous circuit is disclosed whereby processing of the circuit is not directly correlated to a time-periodic event, such as a clock. (see Specification Page 2, Lines 5-8) Therefore, an asynchronous integrated circuit is an integrated circuit that operates in an asynchronous manner. This disclosure is within the description of the related art section of the Applicant specification and is considered appropriate for any asynchronous type operating integrated circuit. The Klughart prior art discloses an integrated circuit that operates in an asynchronous manner, which is equivalent to applicant's invention. (see Klughart col. 16, lines 49-53: IC circuit; col. 37, lines 30-35: asynchronous operation) This equivalent operation discloses an integrated circuit that performs operations including required operations (such as voltage fluctuations, led fluctuations) intended to deceive external observation attempts to discover IC circuit operations.


The Kash and Klughart prior art combination discloses the modification of a power supply voltage utilizing asynchronous operations. (see Klughart col. 22, lines 26-30; col. 37, lines 30-33: supply voltage modulated (regulated, modified))

The examiner has considered applicant's remarks concerning an asynchronous operating integrated circuit, whereby the random variation of the supply voltage causes a time jitter in the processing of the individual operations within the circuit, and any attempts to discover the synchronizing of individual measurements in such side channel attacks are successfully prevented. Applicant's arguments have thus been fully analyzed and considered but they are not persuasive.

Applicant's invention is the implementation of external intrusion detection procedures for integrated circuits utilizing asynchronous operations, which are not correlated to the timings of a clock. The Kash prior art discloses the IC procedures to detect and defeat external observation intrusion techniques. The Kash and Klughart prior art combination discloses the additional limitation of asynchronous operations for the aforementioned integrated circuit. (see Klughart col. 16, lines 49-52: IC circuit; col. 22, lines 26-30; col. 37, lines 30-33: power regulate (power supply modification); col. 34, lines 42-48: protect from reverse engineering)

After an additional analysis of the applicant's invention, remarks, and a search of the available prior art, it was determined that the current set of prior art consisting of Kash (6,515,304) and Klughart (6,396,137) disclose the applicant's invention.

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10,8,07